System Validation

Course Code: EE-920

Course Description:

This course focuses on the principles, current practices, and issues in IC Design Verification. Starting with the review of basic concepts of Verilog and SystemVerilog, students will be introduced to advanced IP verification concepts in IC Design Verification. Students will be introduced to simple testbench, layered testbench and UVM based verification environments. We will also cover advanced topics related to UVM and Verification IPs (VIPs). Finally, students will be able to write configurable, reusable IP Verification Environment along with code coverage and functional coverage analysis.

Text Book:

1. SystemVerilog For Verification: A Guide to Learning the Testbench Language Features By CHRIS SPEAR Synopsys, Inc.
2. ASIC/SoC Functional Design Verification, A Comprehensive Guide to Technologies and Methodologies. By Ashok B. Mehta

Reference Book:

1. UVM Cookbook, Verification Methodology Online Cookbook. By Mentor Graphics

Prerequisites

ASSESSMENT SYSTEM

Quizzes	10%
Assignments	10%
Project	20%
Mid Terms	30%
ESE	30%

Week No.	Teaching Plan/Topics
1	Introduction to IC Design Verification Introduction to SystemVerilog (SV) SV Data Types & Arrays in IC Verification
2	Procedural Statements and Flow Control in SV SV Processes (Fork-join, fork-join any/none) Tasks and Functions in VIP
3	Typedefs, Enums, shallow/deep copy in SV SystemVerilog Classes for Layered Testbench Encapsulation and Extern methods in SV Classes

4	Randomization & Constraints in IP Verification IPC (Inter-process Communication) between testbench components Semaphores and Interfaces in SV
5	DPI (Direct Programming Interface) in SystemVerilog Importing “C” functions in SV Testbench Writing Assertions in SV
6	SVA Sequences for IP verification Functional Coverage and Code Coverage (Line, Toggle, FSM, Assert)
7	SV Based Layered Testbench Architecture Design
8	Introduction to UVM UVM Testbench Hierarchy UVM Phases and UVM Config db
9	**Mid Semester Exam**
10	UVM Sequence Items for IC Verification UVM Sequences & Sequencer Creating UVM Driver, and Monitor
11	Creating UVM Agent Connecting Driver and Sequencer in VIP UVM Test, Environment for IC/SoC
12	UVM Testbench Top UVM Scoreboard UVM Macros
13	Complete UVM Test bench for an IP Code and Functional Coverage report of Verification IP (VIP) UVM Virtual Sequencer and Sequences
14	UVM Subscriber Class Running Directed Tests using UVM Random Testing using UVM
15	APB VIP Testbench Coverage Report for APB VIP
16	Wishbone Slave VIP Testbench Coverage Report for Wishbone Slave VIP
17	Research Project Presentations
18	**End Semester Exam**